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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/064,474	04/22/98	ROY S	TRA-040

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EXAMINER	
WHITMORE,S	
ART UNIT	**PAPER NUMBER**
2783	6

DATE MAILED: 11/24/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/064,474	Subhash et al.
Examiner	**Group Art Unit**
Stacy Whitmore	2783

☒ Responsive to communication(s) filed on *Sep 13, 1999*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-21 and 23-25* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-5, 11-15, 19-21, and 23-25* is/are rejected.

☒ Claim(s) *6-10 and 16-18* 4/4/23 is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. Claims 1-25 are presented for examination.

2. It is noted that the present application does not contain line numbers in the specification of claims, and does not correspond to the preferred format. The preferred format is to number each line of every claim, with each claim beginning with line 1. For ease of reference by both the Examiner and Applicant all future correspondence should include the recommended numbering.

Claim Objections

3. Claim 23 is objected to because of the following informalities: Claim 23 should now depend from claim 21. Appropriate correction is required.

Claim Rejections - 35 U.S.C. § 112

4. Claims 4, 14, and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The claim language in the following claims is not clearly understood:

I. As per claims 4, 14, and 23, it is unclear exactly what is meant by "indication whether or not an instruction has been executed since a previous processor cycle". (Does this mean that information about each instruction is updated when an indication is given that an instruction has or has not been executed or does this mean that the information about each instruction is updated which includes information that an instruction has or has not been executed? explain.)

5. Claims 1, 2, 5, 11-12, 15, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Folwell et al. (5,473,754) in view of Kaneko (5,440,700).

6. Folwell et al. Was cited in a prior office action, paper number 4, dated 6/10/99.

7. As for claim 1, Folwell et al. taught the invention substantially as claimed, including a processor having a real time debugging interface (abstract), comprising:

a) instruction memory means (fig. 2, element 21),

b) program counter means (col. 5, lines 4-5),

c) cause register means for indicating information regarding interrupts and exceptions (col. 5, lines 1-10, and Table 4), and

d) first decoder means for indicating information about an instruction executed by the processor during a clock cycle (fig. 2, element 22),

the first decoder coupled to the instruction memory (fig. 1, elements 21-22, and the cause register, where the first decoder has a first output providing information regarding activity of the processor (fig. 2, elements 24 and 26, fig. 4, elements 52, 53, and 54, col. 1, lines 62-67, col. 2, lines 1-4).

Folwell et al. does not specifically teach the first decoder coupled to the program counter. However, Kaneko disclosed the program counter coupled to a decoder (col.4, lines 30-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Folwell et al. and Kaneko because it would allow for a means of maintaining status in the debugging process (see Kaneko, col. 2, lines 27-33).

Folwell et al. does not specifically teach the decoder operating in real time. However, Folwell et al. did disclose the decoder operating directly with instruction flow and the debug port, both of which operate in real time (see abstract, lines 12-19, col. 2, tables 1-3, and col. 4, lines 55-57). It would have been obvious for one of ordinary skill in the art at the time the invention was made that Folwell et al.'s decoder operates in real time because it is part of normal program operation which operates in real time.

8. As for claim 11, Folwell et al. taught the invention substantially as claimed, including the limitations as cited in claim 1. Folwell et al. Did not specifically disclose plural elements within an embedded system. However, Folwell et al. disclosed his debug device coupled to a host work station via a SCSI bus (fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a plurality of elements in an embedded system into Folwell et al.'s system because Folwell et al.'s system was expandable via the SCSI.

9. As for claims 2, and 12, Folwell et al. taught the information about processor activity includes information as to at least one of a jump instruction has been executed (col. 2 table 3), a jump instruction based on the contents of a register has

been executed (col. 2, table 3), a branch has been taken (col. 2, table 2), and an exception has been encountered (col. 5, table 4).

10. As for claims 5 and 15, Folwell et al. did not specifically teach the first output is a three bit parallel output. However, Folwell et al. disclosed a parallel output of more than three bits (fig. 2, elements 24 and 26). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Folwell et al.'s performed the same function as claimed by applicant because Folwell et al.'s parallel output included at least three bits of information and could have been designed to use three bits as an output.

11. As for claims 19, Folwell et al. disclosed the processor is on a chip having a plurality of pins (col. 1 lines 5-9), and the first output and data output are provided via some of the pins (fig. 1, element 25 and fig. 2, element 26).

12. As for claims 20, Folwell et al. disclosed the first output is an n-bit parallel output (fig. 2, element 26), and the data output is a serial output (see as cited in paragraph 15).

13. Claims 3, 13, 21, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Folwell et al. (5,473,754) in view of Ueki (5,428,618).

14. As for claim 21, Folwell et al. taught a method of debugging a processor comprising:

a) providing information about processor activity in real time (abstract), and

b) associating the instructions executed by the processor with information about processor activity (col. 5, lines 52-53),

Folwell et al. did not disclose wherein said step of providing information about processor activity includes providing information about every instruction executed by said processor.

However, Ueki et al. disclosed providing information about every instruction executed by said processor (see abstract, lines 11-13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Folwell et al. and Ueki et al. because Ueki et al.'s activity information would improve the integrity of Folwell et al.'s system to be able to backtrack for recoveering an internal state of the system (see Ueki et al., abstract).

15. As for claim 24, Folwell et al. taught the information about processor activity includes information as to at least one of a jump instruction has been executed (col. 2, table 3), a jump instruction based on the contents of a register has been executed

(col. 2, table 3), a branch has been taken (col. 2, table 2), and an exception has been encountered (col. 5, table 4).

16. As for claim 25, Folwell et al. disclosed the second decoder means enables the event history buffer means when the cause register means indicate an event of a change in status of an interrupt line, internal processor exception, or a jump based on the contents of a register (col. 1, line 64 - col. 2, line 3, and col. 8, lines 1 - 9).

17. Claims 3 and 13 are viewed as similar to claims 1, 11, and 21, are rejected for the reasons as cited in the rejections of claims 1, 11, and 21.

18. Claims 4, 14, and 23 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

19. Claims 6-10, and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

20. Applicant's arguments with respect to claims 1-5, 12-13, 15, 19-20, 21, and 24-25 filed 9/13/99, have been fully considered but are not deemed to be persuasive and are moot in view of the new grounds of rejection.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Stacy Whitmore, whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday and alternate Fridays from 6:30AM - 4:00PM. The group fax number is (703) 306-5404.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Meng Ai T. An*, can be reached on *(703) 305-9678.*

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Stacy Whitmore
Nov 18, 1999

Meng-Ai T. An
Supervisory Patent Examiner
Technology Center 2700